19.9 A 14mW Fractional-N PLL Modulator with an Enhanced Digital Phase Detector and Frequency Switching Scheme

Mark Ferriss, Michael P. Flynn

University of Michigan, Ann Arbor, MI

The fractional-N frequency synthesizer is a key building block of wireless systems as it can both generate a high frequency signal with a well-defined frequency and modulate that signal [1,2]. This work addresses two limitations of this architecture; the reliance on analog circuitry in deep submicron technology, and the trade-off between low loop bandwidth for good ΔΣ noise rejection and high loop bandwidth for fast modulation rates. A synthesizer is presented that utilizes an all-digital phase detector in place of the conventional analog-intensive phase detector, charge pump and loop filter blocks. In addition, the design uses a digital dual-modulation scheme that alleviates the trade-off between loop bandwidth and switching speed. These techniques are presented as part of a prototype 14mW 2.2GHz MSK transmitter with a transmission rate of 927.5kb/s.

A block diagram of a conventional fractional-N synthesizer is shown in Fig. 19.9.1. The information extracted from the phase detector is inherently analog in nature since the phase information is not synchronized to either the reference clock or the divided down VCO clock and is not quantized. Although conventional XOR and tri-state phase detectors utilize digital building blocks, a charge pump and filter are required to extract useful phase-difference information. Recently, a time-to-digital converter (TDC) is reported that uses multiple flip-flops and unit delays (in practice inverters) to quantize the time difference between the edges of the reference and feedback clock [3]. However, with this approach the resolution and linearity are dependent on the speed and matching of the unit delay elements, and hence inherently process dependent.

If a conventional TDC is analogous to a flash ADC, with the unit delays setting the quantization steps, then the proposed phase detector is analogous to an oversampling ADC, where oversampling and a phase integration loop are used to improve the performance of a coarse single-bit phase quantizer. To achieve this, a unique property of a fractional-N PLL is utilized, that is the ability to control the frequency of the signal coming from the programmable divider by changing the divide ratio.

The new phase detection technique uses a single flip-flop as a phase comparator, while an additional negative feedback loop around the programmable divider keeps the phases of the two clocks aligned to within a single quantization step (Fig. 19.9.2), hence only one comparator (flip-flop) and no inverter delays are required. On the rising edge of the reference clock, the flip-flop samples the divided-down VCO signal, determining whether the divided clock is ahead or behind the reference clock. In this way, the flip-flop effectively acts as a one-bit phase quantizer. This quantized information is then fed back to the input of the ΔΣ modulator that controls the programmable divider, forming the new feedback loop. Changing the divide ratio changes the frequency of the signal coming out of the divider. Because phase is the integral of frequency, this change in frequency forces the fed-back signal to become aligned in phase with the reference clock.

From a phase perspective the new feedback loop incorporates an integrator in its feedback path, hence the phase transfer function between the VCO ($_{vco}$ in Fig. 19.9.2) and the flip-flop output is now high-pass instead of all-pass. Similarly, the transfer function between the frequency control ("Divider ratio" in Fig. 19.9.2) and the flip-flop output becomes all-pass instead of low-pass. A digital integrator at the output of the flip-flop compensates for this. Without a ΔΣ modulator the phase quantization levels would be restricted to the step size of the divider. The presence of the ΔΣ allows the quantization levels to be set arbitrarily small. The new phase detector is almost entirely digital. The only pseudo-analog component is the decision making flip-flop which has requirements similar to a comparator in an ADC. This digital approach does not rely on component matching or on any process dependent parameters such as inverter delay.

The wide fractional-N PLL loop bandwidth required for high-speed modulation conflicts with the requirements for suppression of ΔΣ-shaped noise which necessitates a low-bandwidth loop. Pre-emphasis can compensate for the limited loop bandwidth [4] but requires precise knowledge of the analog characteristics of the loop. Another method is two point modulation, that is adding a signal directly at the input of the VCO, in addition to modifying the divide ratio. However, unless the value of the injected signal exactly matches the VCO gain, the frequency step size will be incorrect.

In the new scheme, the frequency switching rate is not limited by the bandwidth of the loop. Consider the case when the loop is to switch between two different frequencies, A and B, such as for MSK, (Fig. 19.9.3) with the loop initialized to the average of A and B. At the end of each bit period the digital value that determines the VCO control is sampled. When switching between two desired frequencies, for example A and B, the most recent sampled values for A and B are subtracted from each other. The result of this subtraction ("Delta" in Fig. 19.9.3) is added to the VCO control for frequency A, to give an initial digital VCO control value for frequency B. As the required frequency continues to switch between frequencies A and B, then the sampled value of Delta converges on the correct VCO input difference for the required frequencies A and B. This works provided the VCO transfer function is monotonic. This method represents a compromise that allows fast frequency modulation within a low loop bandwidth, as the frequency switching is not limited by the BW of the loop provided that the loop needs only to switch between a small number of discrete frequencies. This also demonstrates the usefulness of having all the relevant signals in the digital domain.

The prototype transmitter is implemented in a 0.13μm mixed-mode CMOS process and occupies an active area of 0.7mm^2 (Fig. 19.9.7). The tuning range of the VCO is from 1.5 to 2.25GHz, which consists of 20MHz analog tuning range and additional tuning range achieved with the use of digitally switched capacitors. A block diagram of the entire system can be seen in Fig. 19.9.4. The analog section of the loop consists of two DACs, a multiplexer, a VCO, and an output buffer. The DACs and analog controlled VCO could be replaced by a digitally controlled oscillator (DCO). The digital section is fully synthesized, apart from the programmable divider [5]. The prototype consumes 14mW from a 1.4V supply. Figure 19.9.5 shows the measured output spectrum for a pure synthesized tone and for random data with an MSK data modulation rate of 927.5kb/s. Figure 19.9.6 shows the measured phase noise. The loop bandwidth can be set to 28kHz or 142kHz. A 185.5MHz reference clock is used, which allows the phase detector to be significantly oversampled.

Acknowledgments:
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References:
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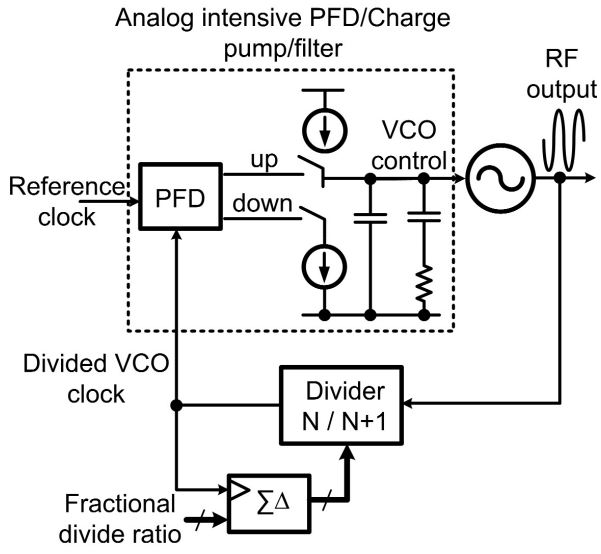

Figure 19.9.1: Conventional fractional-N synthesizer architecture.

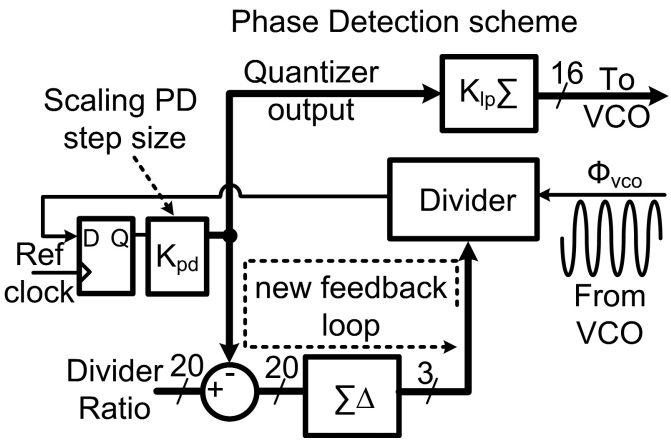

Figure 19.9.2: Digital Phase detector architecture

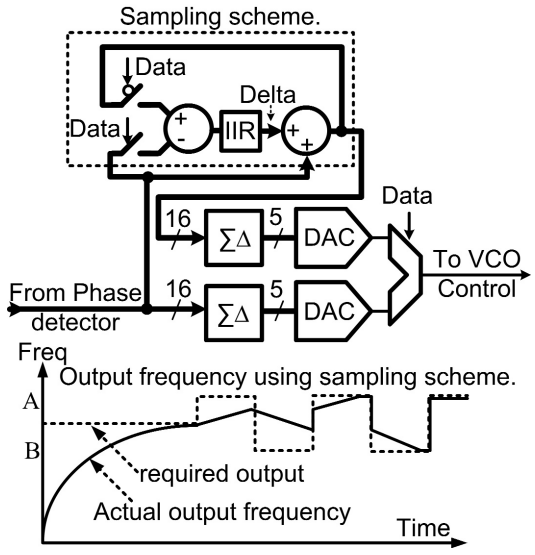

Figure 19.9.3: Sampling scheme at the input of the VCO.

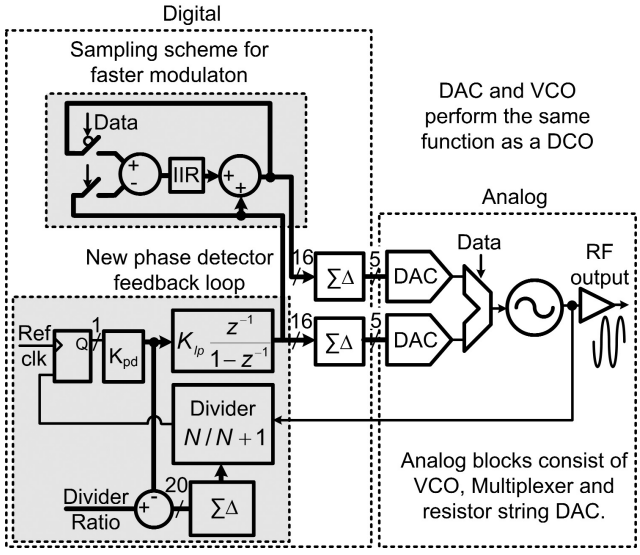

Figure 19.9.4: Complete Architecture.

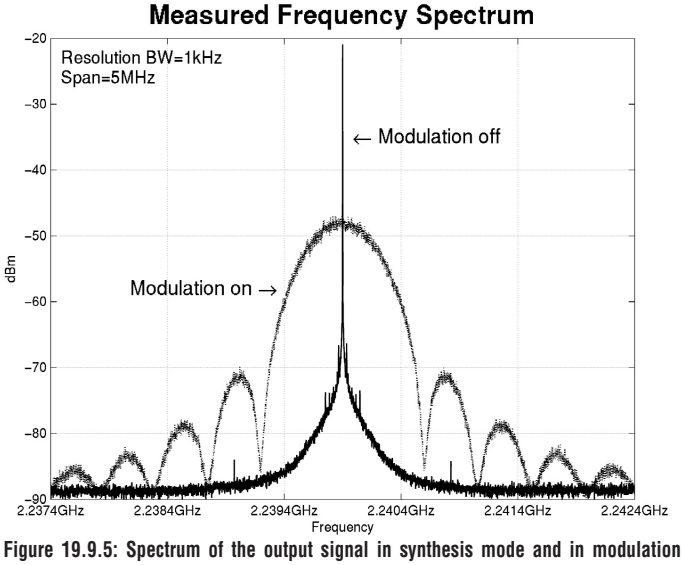

Figure 19.9.5: Spectrum of the output signal in synthesis mode and in modulation mode.

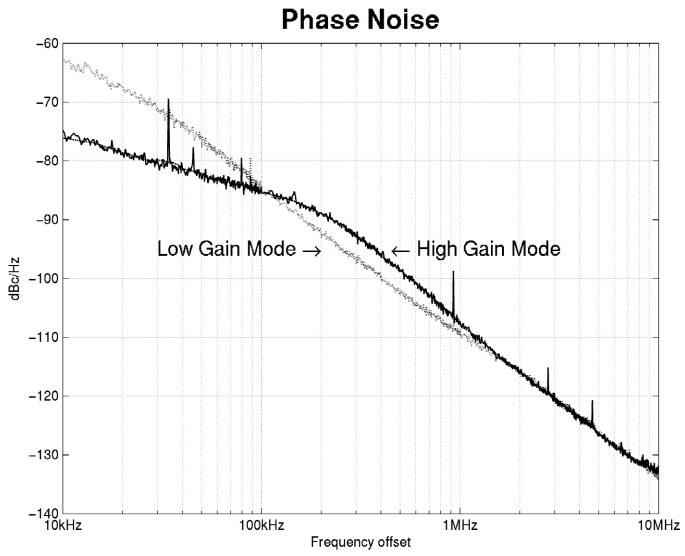

Figure 19.9.6: Phase noise in synthesis mode.

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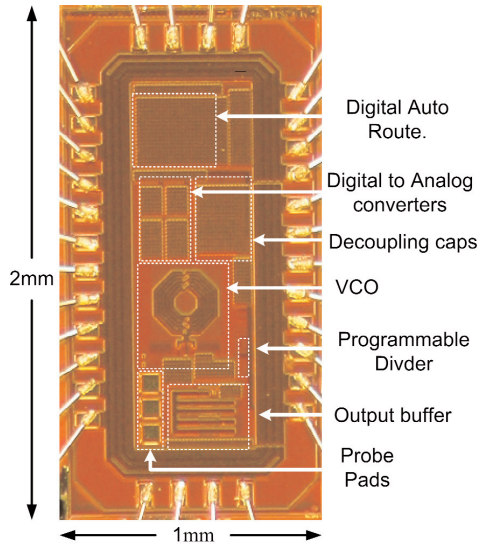

Figure 19.9.7: Die micrograph.

